



Thin-Film Thermal Conductivity Measurements Using Superconducting Nanowires

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Abstract

We present a simple experimental scheme for estimating the cryogenic thermal transport properties of thin films using superconducting nanowires. In a parallel array of nanowires, the heat from one nanowire in the normal state changes the local temperature around adjacent nanowires, reducing their switching current. Calibration of this change in switching current as a function of bath temperature provides an estimate of the temperature as a function of displacement from the heater. This provides a method of determining the contribution of substrate heat transport to the cooling time of superconducting nanowire single-photon detectors. Understanding this process is necessary for successful electrothermal modeling of superconducting nanowire systems.

Keywords Thermometry · Superconductor · Nanowire

1 Introduction

Superconducting nanowire single-photon detectors (SNSPDs) [1] developed for near-infrared wavelengths are an exciting detector technology capable of efficiency exceeding 90% at 1550 nm [2], timing jitter below 5 ps [3], and dark count rates at a few counts per second [4]. By exploiting these properties, SNSPDs have enabled laboratory experiments of quantum sciences [4, 5], improved quantum key distribution [6], and demonstrated optical communication from satellites [7]. Despite laboratory and commercial successes, there are still unresolved questions regarding the fundamental

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physics of SNSPDs. The exact details of the photo-detection mechanism are debated in the literature [8–10], and the precise material properties of common SNSPD materials are not fully understood.

One area of SNSPD theory that has gained attention over the past decade is electrothermal behavior. These models attempt to describe the coupled electrical and thermal behavior of SNSPDs. Electrothermal modeling has been successfully employed to the NbN material system in order to describe device behavior such as latching and afterpulsing [11, 12]. While successful in describing the polycrystalline NbN system, attempts to model the behavior of amorphous WSi embedded in an amorphous SiO₂ dielectric have failed to match experimental measurements. All of these previous modeling attempts have ignored the effect of substrate heating under the assumption that the thermal conductivity of the substrate is sufficiently high to prevent the substrate temperature from changing significantly.

It is commonly known that the thermal transport of thin films differs dramatically from bulk materials. In the Casimir limit, the mean free path of phonons is limited by the thickness of the thin film due to surface scattering and can reduce the thermal conductivity by over order of magnitude compared to the bulk [13]. There is further experimental evidence that the thermal conductivity of thin SiO₂ layers can be reduced even beyond the Casimir limit [14]. With this in mind, it is necessary to reconsider the assumption that substrate heating does not play a role in the electrothermal dynamics of embedded superconducting nanowires.

2 Experimental

2.1 Superconducting Nanowire Thermometry

The development of this thermometry technique is motivated by the desire to better understand the thermal transport in sputtered dielectric thin films without needing to drastically alter the SNSPD fabrication workflow. Arrays of WSi nanowires have been demonstrated where parallel nanowires are fabricated in a co-wound structure [15]. While using normal metal resistors to measure temperature in a noise thermometry or 3ω setup might enable a more accurate measurement, such devices require a different fabrication workflow and additional laboratory readout electronics.

The superconducting nanowire thermometry technique uses the temperature dependence of superconducting nanowire switching currents to determine the temperature of a substrate surrounding the nanowire. An array of parallel superconducting nanowires is fabricated with a single wire acting as the heater while all others act as thermometers. A heater nanowire is biased such that the entire length of the wire is in the normal state and Joule heating in the wire raises the temperature of the substrate surrounding the heater as shown in Fig. 1. The switching currents of the thermometer nanowires are probed under various bias conditions of the heater and correspond to temperatures in the thin film based on the temperature dependence of the switching currents. Calibration curves of this temperature dependence are obtained for each thermometer nanowire by using a heater on the cryostat cold plate to increase the temperature of the device uniformly.

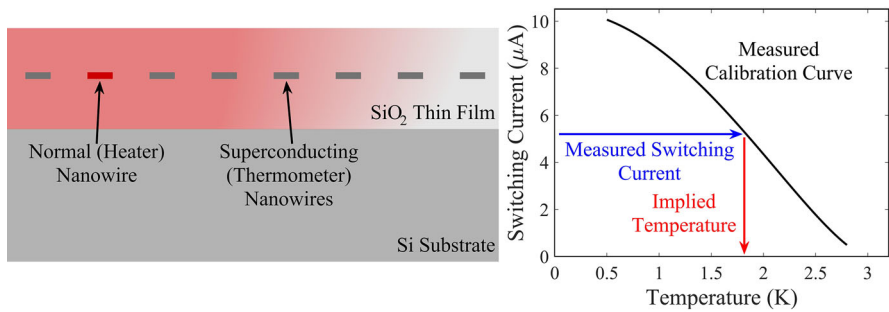


Fig. 1 Superconducting nanowire thermometry scheme. Left shows the cross section of a typical device. A single nanowire is biased in the normal state, heating the surrounding thin film and changing the switching currents of the thermometer nanowires. Right shows how the calibrated switching current curve is used to convert measured switching currents to estimated substrate temperatures surrounding each thermometer nanowire (Color figure online)

2.2 Device Design

Nanowire arrays were fabricated from 5-nm-thick WSi films sputtered from a compound target on a four-inch Si wafer with 240 nm of thermal oxide. Sixteen parallel 160-nm-wide and 270-μm-long nanowires were patterned with electron beam lithography to act as the heater and thermometers. The length ensures a uniform 2D temperature profile in the active region of the device. After patterning, the nanowires were passivated with 110 nm of sputtered SiO₂. Devices were fabricated with 1600- and 400-nm nanowire pitches to understand the thermal transport at different length scales. Inductors were patterned in series with the active region of the nanowire in order to slow the reset time of the nanowires and prevent latching, which would reduce the switching current of the nanowires [16].

2.3 System Model

As the motivation for this experiment is to determine an appropriate model for describing thermal transport in the substrate of SNSPD systems, we use a simple diffusion and boundary resistance formulation for describing the heat flow in the device. Due to its large thermal conductivity, the silicon substrate is approximated to have a uniform temperature T_{Si} which can be elevated above the bath temperature T_{bath} due to interfacial resistance between the silicon die and the gold-plated copper plate. A Cernox thermometer and resistive heater are used to stabilize the bath temperature at a fixed value for the measurements. Diffusion in the SiO₂ layer is modeled according to the simple kinetic formula of the thermal conductivity given by Eq. (1).

$$\kappa_{\text{SiO}_2}(T) = \frac{1}{3} \nu l(T) C(T) \quad (1)$$

In this form, ν is the phonon mode-averaged sound velocity, $l(T)$ is the phonon mean free path, and $C(T)$ is the heat capacity. The mean free path is split into two

contributions according to $l^{-1}(T) = l_{\text{bulk}}^{-1}(T) + l_0^{-1}$ where $l_{\text{bulk}}(T)$ describes the phonon mean free path determined by the same mechanisms that govern the bulk thermal conductivity and l_0 is the temperature-independent mean free path specific to a thin film. The temperature-dependent bulk mean free path is estimated from literature values of the bulk thermal conductivity and heat capacity according to Eq. (2).

$$l_{\text{bulk}}(T) = \frac{3\kappa_{\text{Bulk}}(T)}{vC(T)} \quad (2)$$

The interfacial boundary resistance between the SiO_2 and Si is modeled according to a Kapitza boundary with a boundary condition given by Eq. (3).

$$\kappa_{\text{SiO}_2}(T) \nabla T \cdot \hat{n}|_{\text{interface}} = -R_1(T^{r_1} - T_{\text{Si}}^{r_1}) \quad (3)$$

The fitting parameters R_1 and r_1 are used to model the boundary resistance with the expectation that r_1 equals four according to the acoustic mismatch model. The interface between the silicon and gold-plated copper sample mount is bonded with GE Varnish, leading to a boundary resistance and silicon temperature with the form of Eq. (4).

$$T_{\text{Si}} = \left(\frac{P_{\text{total}}}{R_2} + T_{\text{bath}}^{r_2} \right)^{1/r_2} \quad (4)$$

The fitting parameters R_2 and r_2 are used to model the boundary resistance and P_{total} is the total heat dissipated in the heater nanowire. The Kapitza boundary between the SiO_2 and Si is expected to have the same behavior for both the 1600-nm-pitch and 400-nm-pitch devices. However, because the two separate dies were mounted at different times on the sample mount, the fitting parameters used to model interfacial boundary resistance between the silicon and copper plate are expected to change. The fitting parameters are the SiO_2 frequency-independent mean free path, SiO_2 –Si Kapitza boundary parameters, and the silicon temperature parameters. Thermal energy from the heater nanowire is introduced as a time-independent heat source. The thermal conductivity differential equation and boundary conditions are solved using COMSOL to find a steady-state temperature distribution.

3 Results

Nanowires were biased with a low noise voltage supply and bias resistor in series with the nanowire. The current was calculated by dividing voltage across the bias resistor by the bias resistance. Current–voltage curves of the heater nanowire were used to extract the total power dissipation at a given bias condition, the power dissipated per unit length of the nanowire, and the square resistance of the nanowire in the normal state. Thermometry data were measured for heater powers ranging 1.9–23 nW/ μm for the 1600-nm-pitch device and 0.7–11 nW/ μm for the 400-nm-pitch device.

The thermometry results were fitted to the heat transfer model described above to estimate the thermal conductivity and Kapitza boundary resistance properties of the

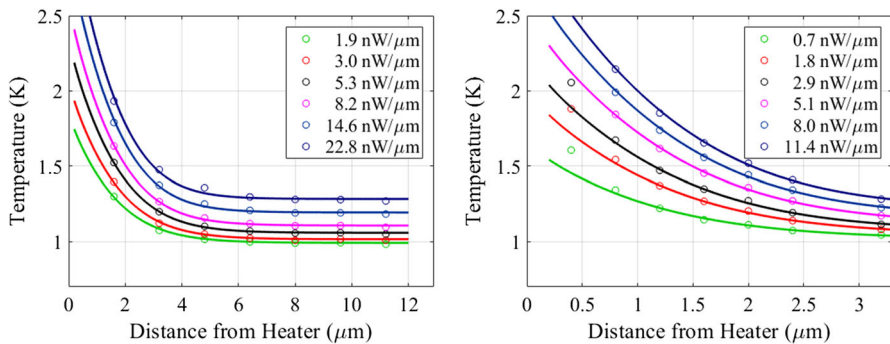


Fig. 2 Experimental data and modeling fits. Circles indicate the measured data while the lines are the model fit. Left shows the 1600-nm-pitch data taken with a bath temperature of 950 mK. There is a reasonable fit for all data points when using the fit parameters $l_0 = 180.2$ nm, $r_1 = 5$, $R_1 = 66.1$ W/m²K⁵, $r_2 = 4$, and $R_2 = 3.70$ W/K⁴. Right shows the 400-nm-pitch data taken at a bath temperature of 1000 mK. The fitting parameters are $l_0 = 96.7$ nm, $r_1 = 5$, $R_1 = 66.1$ W/m²K⁵, $r_2 = 4$, and $R_2 = 2.92$ W/K⁴. No set of fitting parameters is able to match all of the experimental data for the 400-nm-pitch device (Color figure online)

SiO₂ films. The best fit to the data required a SiO₂–Si Kapitza power r_1 of approximately 5 rather than the expected 4 based on the acoustic mismatch model. The optimized fits with fixed parameters of $r_1 = 5$, $R_1 = 66.1$ W/m²K⁵, and $r_2 = 4$ are shown in Fig. 2. The 1600-nm-pitch data model matches the experimental data for all thermometry data points, while the 400-nm-pitch data cannot be reproduced for the thermometry data nearest to the heater.

Fitting the model to the two data sets shows that the fixed frequency mean free path varies significantly between the 400-nm-pitch and 1600-nm-pitch devices. For the 1600-nm-pitch results, the thermal conductivity is approximately 51% of the expected Casimir limited thermal conductivity based on the total thickness of the SiO₂ layer. In contrast, the 400-nm-pitch results show a thermal conductivity significantly smaller at 28% of the expected Casimir limit. This result is consistent with the trend of the literature reported values of the thermal conductivity of SiO₂ in thin films [13]. The drop in thermal conductivity can be understood as decreasing the mean free path of phonons due to the increased density of nanowires in the film which act as scattering surfaces for the phonons. This effect dominates any potential increase in conductivity due to the presence of the metal due to the small thickness fraction of the nanowire compared to the dielectric and the Kapitza boundary between metal and dielectric.

4 Conclusion

Our nanowire thermometry experiments indicate that the effective thermal conductivity of the SiO₂ thin films used in the optical cavities of SNSPDs is significantly smaller than the bulk thermal conductivity and even smaller than the Casimir limited thermal conductivity expected from boundary scattering at the film interfaces. The effects of substrate heating are currently neglected in electrothermal models of nanowire systems, but based on these measurements, the substrate temperature can

increase significantly at the power dissipation levels seen in SNSPD operation. As an approximate example, if the inductive energy ($LI^2/2$) of a typical WSi single pixel biased at 8 μA with an electrical reset time constant of 25 ns is dissipated in a rise time of 2 ns over a 2 μm hotspot length, the corresponding power dissipation is 10 nW/ μm . While the model presented above improves upon the description of the substrate in an SNSPD, it inadequately describes the energy transfer within the SiO_2 thin film near the heater nanowire, as seen by the deviation from experiment. This may be due to additional fluctuations which suppress the switching current of the adjacent probe nanowire. Furthermore, the model does not consider any transient effects present on the nanosecond timescales relevant to thermal dissipation during a detection event. At the cost of significant complexity, a model based on the Boltzmann transport equations [17, 18] may be necessary to resolve these shortcomings. Despite the model's current limitations, our experiments suggest that an accurate electrothermal model capable of predicting the hot spot current and latching behavior of SNSPDs must consider the effects of substrate heating when wires are embedded in dielectric thin films.

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